The AMD Athlon™ Processor: Architectural Enhancements for Advanced Multiprocessor Systems

Microprocessor Forum

October 2000

Overview

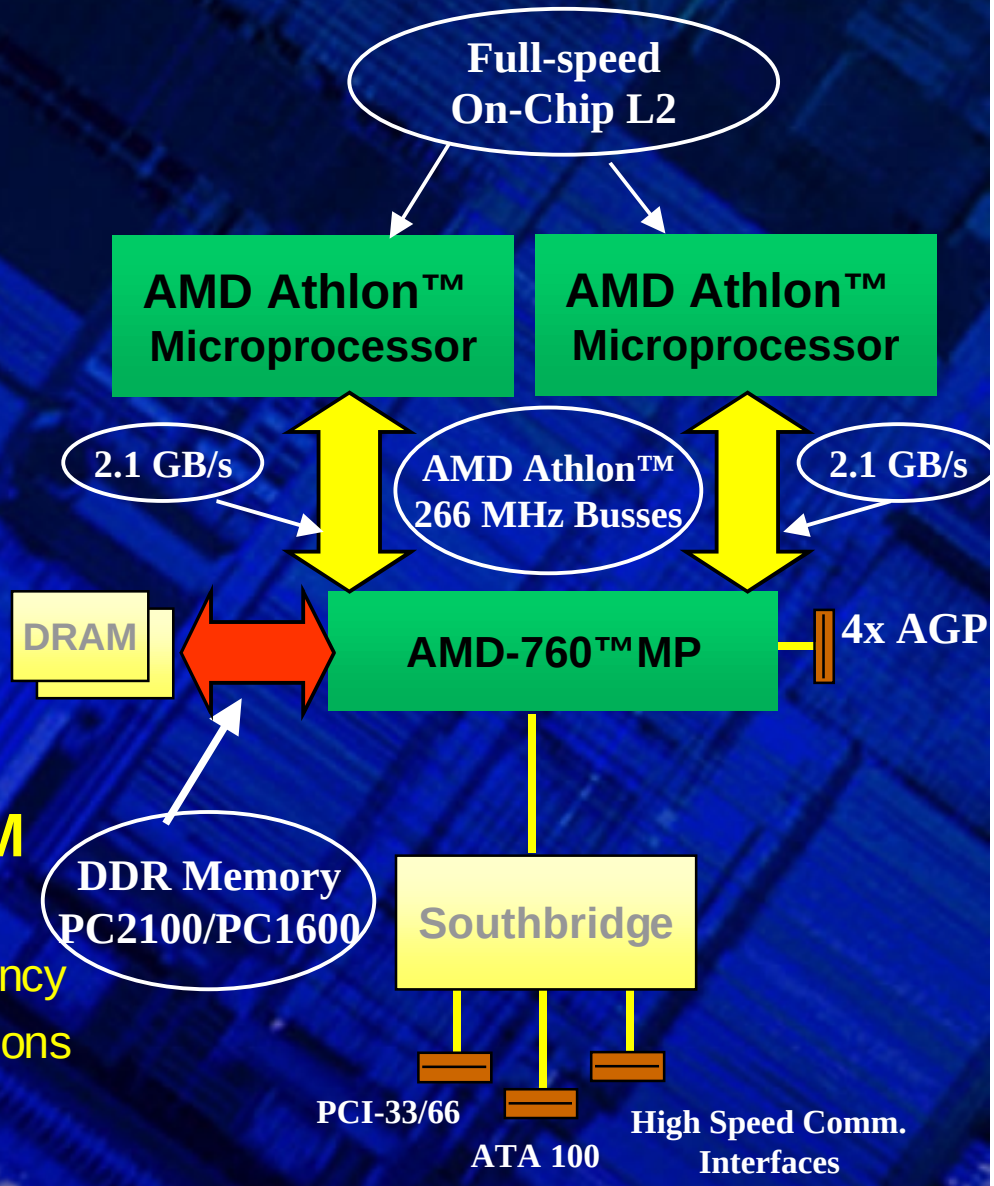
- **The AMD Athlon™ processor and the AMD-760™MP chipset enable the next generation of high performance x86 multiprocessing systems**
  - 7th Generation microprocessor core
  - AMD multiprocessing chipset
- **Together, the AMD Athlon™ processor, AMD-760™MP chipset, and DDR memory technology provide relief from bottlenecks associated with existing x86 multiprocessing systems**
  - Exclusive cache architecture
  - Point-to-Point FSB transfers
  - PC2100 DDR memory technology

The Ideal SMP System Model: *In a Perfect World*

- **Microprocessor Core**
  - Superscalar Floating-point Engine for computational intensive applications
  - On-die, full speed Advanced Cache Subsystem
- **Processor Front-Side Bus (FSB)**
  - Bus protocol designed for scalable multiprocessing
  - High bandwidth topology between processor, memory, graphics, and peripherals
  - Snoop traffic does not impact performance
- **Memory Subsystem**
  - High bandwidth, low latency memory technology
  - Cost-effective
  - Widely Available
- **Chipset**
  - Maximum memory bandwidth for processors and graphics to system memory
  - Maximum system transaction concurrency
  - More efficient memory coherency protocol

AMD Athlon™ Platform: *Bandwidth Realization*

- **AMD Athlon™ Processor**
  - Superscalar Floating Point Engine
  - On-die, full speed advanced cache subsystem with:
    - Exclusive cache architecture
    - Largest L1 cache (128kB)
    - Large L2 caches (256+kB)
- **Processor Front-Side Bus**
  - Point-to-Point (non-sharing) topology
    - Optimized and scalable MP bus protocol
  - Dedicated Snoop bus
- **PC2100 & PC1600 DDR SDRAM Memory**
  - High Bandwidth (2.1 GB/s) and low latency
  - Available and cost-effective for all solutions
- **AMD-760™ MP Chipset**
  - Two 266MHz (2.1 GB/s) AMD Athlon™ processor FSBs

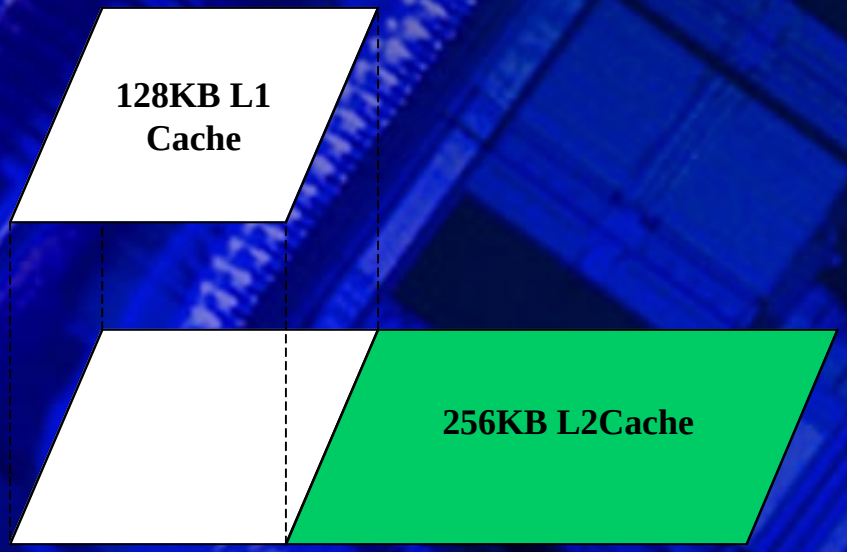


L2 Cache: Exclusive vs. Inclusive

AMD

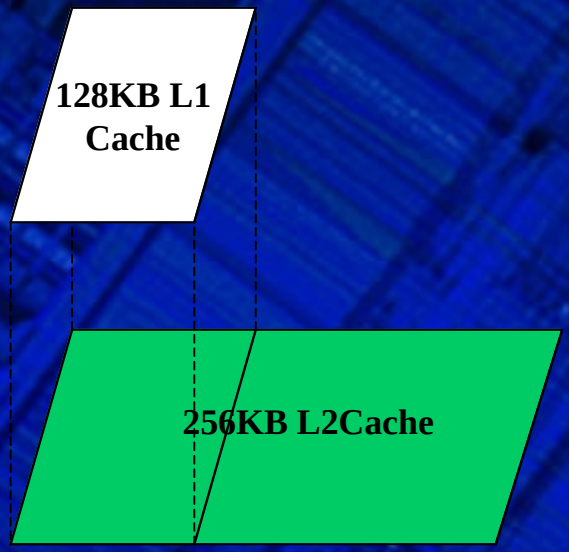
AMD Athlon™ Processor

Exclusive



Total Size = 256KB L2 + 128KB L1 = 384KB

Inclusive

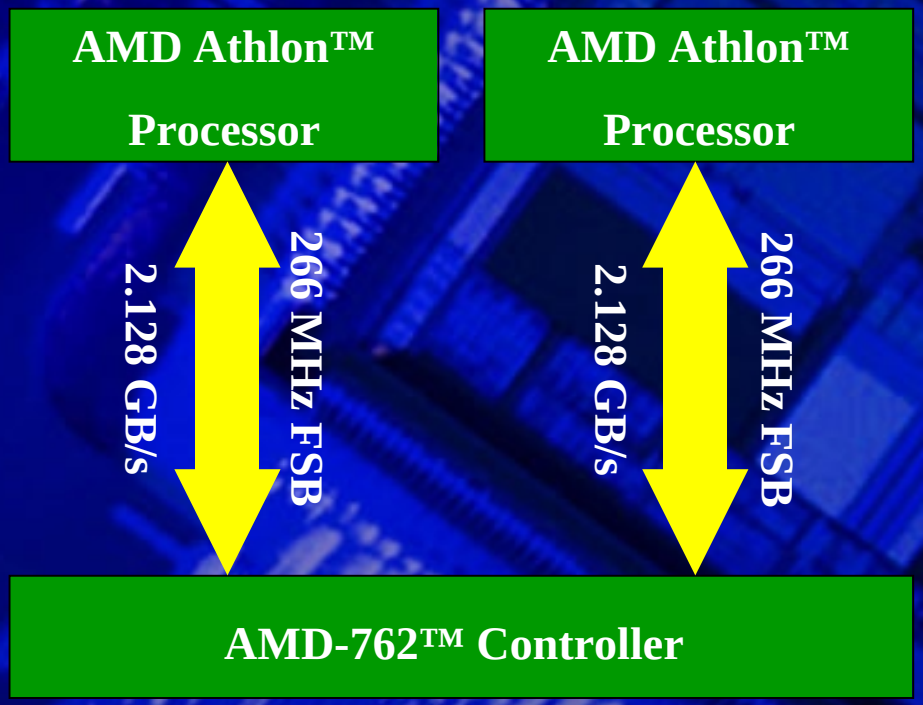


Total Size = 256KB L2 +/- 128KB L1 = 256KB

- Greater effective cache size from exclusive architecture with the AMD Athlon™ processor.
- Dedicated L1 snoop port to service probe requests without interfering with L1 loads and stores.

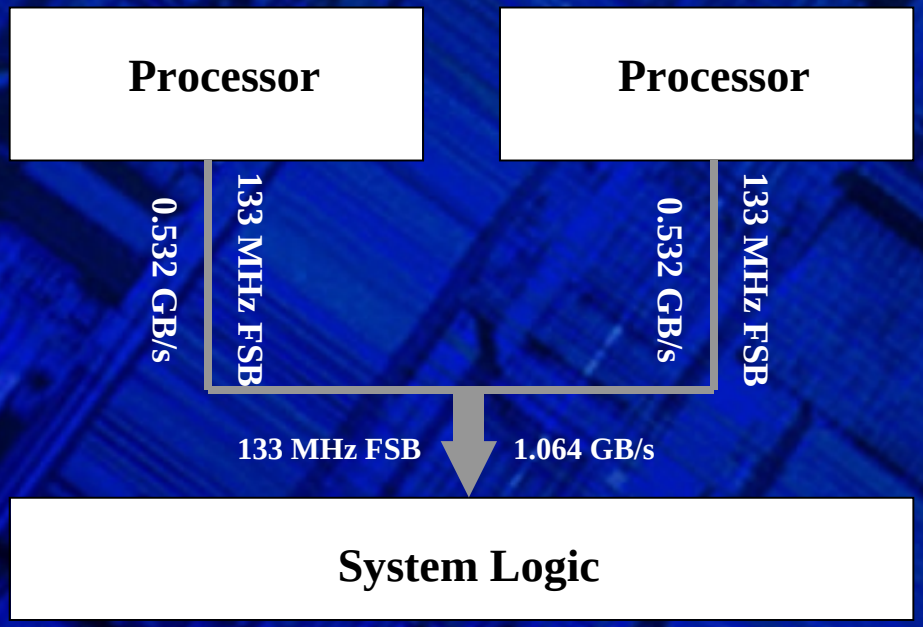
Point-to-Point vs. Shared Bus

POINT-TO-POINT



- 2.1 GB/s per processor
- 4.2 GB/s Total Bandwidth

SHARED BUS



- 532 MB/s per processor (1.064 / 2)
- 1.064 GB/s Total Bandwidth

DDR is an Evolutionary Upgrade

- **PC2100 DDR provides over 2.1GB/s bandwidth**
- **Cost-effective**
  - Similar protocols and design methodologies to SDRAM
  - JEDEC standard I/O drivers
  - Same manufacturing infrastructure
  - Standard TSOP packaging
- **Serves all markets**
- **Available from leading vendors**

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- **Together, the AMD Athlon™ processor, AMD-760™MP chipset, and DDR memory technology provide relief from bottlenecks associated with existing x86 multiprocessing systems**
  - Exclusive cache architecture
    - Greater effective cache size
    - Dedicated snoop port
  - Point-to-Point FSB transfers
    - System bandwidth realization and utilization
  - PC2100 DDR memory technology
    - High bandwidth and low latency in a cost-effective and widely available solution

For All of Your Workstation and Server Needs